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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MONDT, JOHANNES P	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 02/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/664,094	MIZUNO, MASAYUKI	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5 and 9-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5 and 9-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Amendment filed 11/12/2004 forms the basis of this office action. In said Amendment Applicant substantially amended claims 9 and 11 and added new claims 13-15. Claims 1, 2, 5, 9, 10, 11 and 13-15 are pending.

Comments on Remarks in said Amendment are included below under "Response to Arguments".

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claim 2 and 11*** are rejected under 35 U.S.C. 103(a) as being unpatentable over McCorkle (5,523,728) in view of Lin et al (6,225,568), or, - in the alternative: over MacDonald (5,633,613) (made of record and cited previously) in view of Lin et al (6,225,568).

McCorkle teaches (Figures 1-6, especially Figure 6(c)) a semiconductor integrated circuit (see abstract) comprising: a signal line 41 (col. 6, l. 56-57); a ground plate 45 (col. 6, l. 59) and another signal line 51 (col. 6, l. 54-55) disposed on an opposite side (cf. Figures 1 and 6(c) and col. 6, l. 46-61) of said ground plate (Figure 6(c)) as said signal line.

Similarly, MacDonald teaches a semiconductor integrated circuit comprising a signal line 30, a ground plate 34 and another signal line 32 disposed on an opposite side (cf. Figure 1) of said ground plate as said signal line 30 (cf. col. 3, l. 11 –48).

McCorkle nor MacDonald necessarily teach the limitation that at least one through hole is formed in said ground plate and an inner wall of said through hole only directly electrically connected to said ground plate wherein an aperture size of said through hole is smaller than a width of said signal line. *However, it would have been obvious to include said limitation in view of Lin et al*, who, in a patent application drawn to a circuit board having shielding planes in transmission mode circuits with transmission lines, - hence closely related to the inventions by McClorke and MacDonald, teach the ground plates to have at least one (in fact a plurality) through hole formed in the ground plate, an inner wall of said through hole being only directly electrically connected to said ground plate (by virtue of being a void) (see col. 6, l. 10-58) and wherein an aperture size of said through hole is smaller than a width of said signal line. Said at least one through hole is included for the specific purpose of reducing the signal line capacitance (loc.cit.) and the impedance (see abstract). *Motivation* for the inclusion of the teaching by Lin in the invention by McClorke or in the invention by MacDonald derives from the resulting improved impedance of the transmission lines, thereby allowing control of the transmission timing (see abstract and col. 3, l. 47 – col. 4, l. 10).

On claim 11: McCorkle teaches (Figures 1-6, especially Figure 6(c)) a semiconductor integrated circuit (see abstract) comprising: a signal line 41 (col. 6, l. 56-

57); a ground plate 45 (col. 6, l. 59) and another signal line 51 (col. 6, l. 54-55) disposed on an opposite side (cf. Figures 1 and 6(c) and col. 6, l. 46-61) of said ground plate (Figure 6(c)) as said signal line.

Similarly, MacDonald teaches a semiconductor integrated circuit comprising a signal line 30, a ground plate 34 and another signal line 32 disposed on an opposite side (cf. Figure 1) of said ground plate as said signal line 30 (cf. col. 3, l. 11 –48).

McCorkle nor MacDonald necessarily teach the limitation that a plurality of through holes is formed in said ground plate and an inner wall of said plurality of through holes is only directly electrically connected to said ground plate, wherein said plurality of through holes are formed along a longitudinal direction of a signal transmission line and arranged at equal spaces or in a same pattern, and wherein an aperture size of said plurality of said through holes is smaller than a width of said signal line.

However, it would have been obvious to include said limitation in view of Lin et al, who, in a patent application drawn to a circuit board having shielding planes in transmission mode circuits with transmission lines, - hence closely related to the inventions by McClorke and MacDonald, teach the ground plates to have a plurality of through holes formed in the ground plate, an inner wall of said plurality of said through holes being only directly electrically connected to said ground plate (by virtue of being a void) (see col. 6, l. 10-58), wherein said plurality of through holes are formed along a longitudinal direction of a signal transmission line (see Figure 2 and col. 6, l. 44 – col. 7, l. 40), and wherein an aperture size of said through hole is smaller than a width of said

signal line (Figure 2). Said plurality of through holes is included for the specific purpose of reducing the signal line capacitance (loc.cit.) and the impedance (see abstract). *Motivation* for the inclusion of the teaching by Lin in the invention by McClorke or the invention by MacDonald derives from the resulting improved impedance of the transmission lines, thereby allowing control of the transmission timing (see abstract and col. 3, l. 47 – col. 4, l. 10).

3. ***Claims 1, 9, 10, 14 and 15*** are rejected under 35 U.S.C. 103(a) as being unpatentable over McClorke (5,523,728), in view of Heckaman et al (4,851,793), or, - in the alternative over MacDonald (5,633,613) in view of Heckaman et al (4,851,793).

McClorke teaches (Figures 1-6, especially Figure 6(c)) a semiconductor integrated circuit (see abstract) comprising: a signal line 41 (col. 6, l. 56-57); a ground plate 45 (col. 6, l. 59) and another signal line 51 (col. 6, l. 54-55) disposed on an opposite side (cf. Figures 1 and 6(c) and col. 6, l. 46-61) of said ground plate (Figure 6(c)) as said signal line.

Similarly, MacDonald teaches a semiconductor integrated circuit comprising a signal line 30, a ground plate 34 and another signal line 32 disposed on an opposite side (cf. Figure 1) of said ground plate as said signal line 30 (cf. col. 3, l. 11 –48).

McClorke nor MacDonald necessarily teach the limitation defined by the final three lines of claim 1 nor of the final four lines of claim 10. *However, it would have been obvious to include* said limitations in view of *Heckaman et al*, who in a patent on a transmission line parallel to a ground plate designed to select its impedance, hence closely related to the inventions by McClorke and MacDonald, and for the specific

purpose to create a signal line with a single spatial periodicity defining the characteristic impedance (see Abstract), to have at least one through hole (mesas 14) formed in said signal line (here 11) (thus meeting claim 1 in this regard), in fact a plurality of through holes 14 (loc.cit.) (thus meeting claim 10 in this regard) and an inner wall of said plurality of through holes is only directly electrically connected to said signal line (thus meeting claim 1 in this regard), respectively directly electrically connected to said signal line (here signal line 11; col. 3, l. 40- -col. 4, l. 12) (thus meeting claim 10 in this regard) (cf. col. 3, l. 40 – col. 4, l. 12; please note that the dielectric jacket itself is not conductive), wherein an aperture size W_m of said through hole is smaller than a width of said signal line, i.e., than a width of said signal line 11 (thus meeting claim 1 in this regard as well as the further limitation as defined by claim 14 as dependent upon claim 10), and wherein said plurality of through holes are formed along a longitudinal direction of a signal transmission line and arranged at equal spaces or in a same pattern (the channel directions define the longitudinal direction in light of the specification, while the regularity of the pattern follows from the single value of both W_m and W_c yielding a single periodicity (see abstract and col. 3, l. 53-64)). *Motivation* to include the teaching by Heckaman et al in both claims 1 and 10 derives from the possibility to thereby define the characteristic impedance of the signal line. It is noted that only the teaching of the waffle-like constitution of the signal line needs to be adopted from Heckaman et al, which is no way affects the other aspects of McClorke and MacDonald as it pertains to the invention as claimed.

On claim 9: the pre-amble and first three lines of the bulk of this claim are identical to the pre-amble and first three lines of the bulk of claim 1, which, as mentioned is taught by McClorke and also by MacDonald. Although neither McClorke nor MacDonald necessarily teach the limitation as defined by lines 4-8 of the bulk of claim 9, it would have been obvious to include said limitation in view of Heckaman et al, who in a patent on a transmission line parallel to a ground plate designed to select its impedance, hence closely related to the inventions by McClorke and MacDonald, and for the specific purpose to create a signal line with a single spatial periodicity defining the characteristic impedance (see Abstract), to have a plurality of holes in said signal line comprised of a plurality of strips connected at respective terminal ends of said strips (the terminal ends of said strips are the channels running in one direction, the connection between the strips running in the other direction, out of two orthogonal directions along which the channels 12 are oriented: aforementioned mesas 14 meet the holes (loc.cit.) and the strips are the plate structure 11 in the channels 12 (col. 3, 3, l. 40 – col. 4, l. 12), and an inner wall of said holes is only directly electrically connected to said signal line (said dielectric jacket being non-conductive) (col. 4, l. 6), wherein a width of each of said holes is smaller than a width of the signal line, i.e.: wherein an aperture size W_m of said through hole is smaller than a width of said signal line, i.e., than a width of said signal line 11.

Neither Heckaman nor McCorkle nor MacDonald necessarily teach said holes to be slit holes. However, in light of the specification "slit holes" distinguishes only from the "holes" of the prior art (Heckaman et al) by being elongated rather than square, i.e., only

distinguishes by an infinitesimal difference in the range limitation on the length and width of the mesas 14 in Heckaman et al. Applicant is reminded that it has been held that a *prima facie* case of obviousness typically exists when the range as claimed overlaps the ranges disclosed in the prior art or when the range does not overlap but is close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003). In the instant case, one skilled in the art would not expect any difference in properties because said difference is infinitesimal.

On claim 15: a width of each holes is smaller than a width of each of the respective plurality of thin strips (width of holes = W_M), while the width of the plurality of thin strips is W_M+ 2*$W\gamma$, where $W\gamma = 0.5 * W_C$, which exceeds W_M by a positive amount.

4. ***Claim 5*** is rejected under 35 U.S.C. 103(a) as being unpatentable over McClorke et al (5,523,728) in view of Heckaman et al (4,851,793) and Lin et al (6,225,568), or, - in the alternative, over MacDonald (5,633,613) in view of Heckaman et al and Lin et al (loc.cit.).

McClorke teaches (Figures 1-6, especially Figure 6I) a semiconductor integrated circuit (see abstract) comprising: a signal line 41 (col. 6, l. 56-57); a ground plate 45 (col. 6, l. 59) and another signal line 51 (col. 6, l. 54-55) disposed on an opposite side (cf. Figures 1 and 6I and col. 6, l. 46-61) of said ground plate (Figure 6I) as said signal line.

Similarly, MacDonald teaches a semiconductor integrated circuit comprising a signal line 30, a ground plate 34 and another signal line 32 disposed on an opposite side (cf. Figure 1) of said ground plate as said signal line 30 (cf. col. 3, l. 11 –48).

McClorke nor MacDonald necessarily teach the limitations defined by (a) lines 6-8 of claim 5, nor the limitation defined by (b) lines 9-11 of claim 5. *However,*

Ad (a) it would have been obvious to include said limitation in lines 6-8 of claim 5 in view of *Heckaman et al*, who in a patent on a transmission line parallel to a ground plate designed to select its impedance, hence closely related to the invention by McClorke, and for the specific purpose to create a signal line with a single spatial periodicity defining the characteristic impedance (see Abstract), to have at least one through hole (mesas 14) formed in said signal line (here 11) (thus meeting claim 5 in this regard), in fact a plurality of through holes 14, and an inner wall of said at least one through hole is only directly electrically connected to said signal line (thus meeting claim 5 in this regard) (here signal line 11; col. 3, l. 40- -col. 4, l. 12); please note that the dielectric jacket itself is not conductive). Furthermore, an aperture size W_m of said through hole is smaller than a width of said signal line, i.e., than a width of said signal line 11 (thus meeting claim 5 in this regard).

Motivation to include the teaching by Heckaman et al in claim 5 derives from the possibility to thereby define the characteristic impedance of the signal line. It is noted that only the teaching of the waffle-like constitution of the signal line needs to be adopted from Heckaman et al, which is no way affects the other aspects of McClorke and MacDonald as it pertains to the invention as claimed.

Ad (b), However, it would have been obvious to include said limitation as defined by lines 9-11 of claim 5 in the invention as defined by McClorke/MacDonald and Heckaman et al in view of Lin et al, who, in a patent application drawn to a circuit board having shielding planes in transmission mode circuits with transmission lines, - hence closely related to the invention by McClorke/MacDonald and Heckaman et al, teach the ground plates to have at least one (in fact a plurality) through hole formed in the ground plate, an inner wall of said through hole being only directly electrically connected to said ground plate (by virtue of being a void) (see col. 6, l. 10-58). Said at least one through hole in the ground plate is included for the specific purpose of reducing the signal line capacitance (loc.cit.) and the impedance (see abstract).

Motivation for the inclusion of the teaching by Lin in the invention by McClorke or the invention by MacDonald derives from the resulting improved impedance of the transmission lines, thereby allowing control of the transmission timing (see abstract and col. 3, l. 47 – col. 4, l. 10).

5. ***Claim 13*** is rejected under 35 U.S.C. 103(a) as being unpatentable over McCorkle, Heckaman and Lin et al as applied to claim 5 above, or, - in the alternative over MacDonald, Heckaman et al and Lin et al as applied to claim 5 above, and further in view of Kuroda et al (5,479,138). Although, as detailed above, claim 5 is unpatentable over McCorkle/MacDonald, Heckaman et al and Lin et al, none of whom necessarily teach the further range limitation as defined by claim 13. *However, it would have been obvious to include further limitation (b)* in view of Kuroda et al, who teach in a patent on the reduction of unwanted impedance deviations in a multi-layer wiring board, - hence

closely related art, that the hole size should be selected in a range determined by an inequality satisfied for any hole size between zero and a certain maximum value, said maximum value being determined by:

$R_y <= 25.98\ R_x^{-0.3871} - 4.370$; here R_y is the width of the ground plate divided by the signal line width and R_x is the ratio of the square of the hole size divided by ground plate width expressed in percentage; said inequality is satisfied provided for any given ground plate width and signal width the hole size is small enough, while from Figure 2 it follows that the dependence of the maximum deviation of the impedance on the open area ratio R_x defined above is characterized by a monotonically increasing function: i.e., the lower the open area ratio, the lower the (harmful) maximum deviation of the impedance can be made (cf. col. 3, l. 12-25). Although in the particular examples provided by Kuroda et al the hole size still exceeds the signal width, the teaching by Kurado et al of the entire range implies that the range as claimed and the range as taught by the prior art overlap. Applicant is reminded that a *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

Response to Arguments

1. Applicant's arguments, see Amendment, filed 11/12/2004, with respect to the rejections of claims 1, 2, 5, 9-11 have been fully considered and are persuasive: the rejections under 35 U.S.C. 102 based on Phelan (claim 5) and Fuchida et al (claims 9-11) have been withdrawn because neither Phelan nor Fuchida et al teach a through hole in a *signal line with size smaller than the width of said signal line*, as opposed to ground or power lines. Furthermore, the rejection under 35 USC 103 of claims 1 and 2 have been withdrawn because Kuroda et al only teach the range for the hole size for a ground plate, not for a signal line.

However, upon further consideration, a new ground of rejection is made in view of McCorkle (or in the alternative: MacDonald as made of record) and Lin et al for claims 2 and 11, based on McCorkle (or in the alternative: MacDonald as made of record) and Heckaman et al for claims 1, 10 and 14, based on McCorkle (or, in the alternative: MacDonald as made of record), Heckaman et al and Lin et al for claim 5, and based on McCorkle (or in the alternative: MacDonald as made of record), Heckaman et al, Lin et al and Kuroda et al (Kuroda et al only is applied to the range specifically taught by Kuroda et al for the through hole in the ground plate, to which it specifically is addressed).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
February 4, 2005

Patent Examiner:

Johannes Mondt (Art Unit: 2826)